IFW

Docket No.: 8733.915.00-US
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of: Kyoung Mook LEE et al.	Customer No.: 30827
Application No.: 10/663,774	Confirmation No.: 1766
Filed: September 17, 2003	Art Unit: 2871
For: ARRAY SUBSTRATE FOR LIQUID CRYSTAL DISPLAY AND FABRICATION METHOD THEREOF	Examiner: Prasad R. Akkapeddi

REQUEST FOR RECONSIDERATION

MS Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In response to the Office Action dated March 23, 2005, wherein pending claims 1-30 have been rejected. Applicants respectfully request favorable reconsideration in view of the remarks presented herein below.

In paragraph 2 of the Office Action ("Action"), the Examiner rejects claims 1-5, 7-19 and 23-30 under 35 U.S.C. §103(a) as allegedly being unpatentable over U.S. Patent No. 6,215,541 to Song ("Song") in view of U.S. Patent No. 6,184,947 to Ozaki. Applicants respectfully traverse this rejection.

In order to support a rejection under 35 U.S.C. §103, the Examiner must establish a *prima facie* case of obviousness. To establish a *prima facie* case of obviousness, three criteria must be met. First, there must be some motivation to modify or combine the cited references. Second, there must be a reasonable expectation of success. Finally, the combination must teach

each and every claimed element. In the present case, claims 1-5, 7-19 and 23-30 are rendered unpatentable over the combination of Song and Ozaki because the Examiner fails to establish a *prima facie* case of obviousness as discussed below.

Independent claim 1 defines an array substrate for a liquid crystal display. The array substrate includes, *inter alia*, a gate line and a thin film transistor having a gate electrode, a source electrode, a drain electrode, and an active layer formed over the substrate; an interlayer insulating layer formed on the thin film transistor; a first gate redundancy line formed on the interlayer insulating layer and connected electrically with on of the gate electrode, the gate line, and both the gate electrode and gate line through a first gate contact hole and formed of the same material as one of the source and drain electrodes; a passivation layer provided on the first gate redundancy line and the interlayer insulating layer; and a pixel electrode electrically connected with the drain electrode through the drain contact hole formed in the passivation layer.

In rejecting claim 1, the Examiner asserts that Song discloses an array substrate as claimed, except that Song fails to disclose that the gate redundancy line is formed of the same material as one of the source and drain electrodes. More specifically, the Examiner notes that Song discloses that the gate redundancy line is made of chromium, molybdenum or molybdenum alloy, and the source and drain electrodes are made of a semiconductor material. In addition, the Examiner asserts that Ozaki discloses a gate line can also be made of a semiconductor layer having a high impurity concentration. Therefore, the Examiner concludes that it would have been obvious to one skilled in the art "to adapt the gate line made from a semiconductor material (as taught by Ozaki) in place of metals such as chromium, molybdenum or molybdenum alloy (as taught by Song) to avoid pin holes that might be formed in the metal layers and to repair any breakage in the metal layer." These assertions are unfounded for the following reasons.

First, the Examiner points to FIG. 5, specifically reference numeral 64, of Song as

disclosing a gate redundancy line. However, as clearly discussed in column 5, lines 55-57 and column 6, lines 1-8, reference numeral 64 of FIG. 5 is a *data* line connector, not a *gate redundancy* line as claimed.

Second, the Examiner points to column 3, lines 49-56 of Ozaki as discloses that the gate line can be made of a semiconductor layer. Actually, the cited passage discloses that the gate line is made of a double layer structure, comprising a semiconductor layer having high impurity concentrations *and* a metal bus layer. Nowhere in Ozaki is there any disclosure or suggestion of forming a gate line out of the same material as one of the source and drain electrodes.

Accordingly, even if *arguendo* one skilled in the art were motivated to combine Song and Ozaki, as suggested by the Examiner, the combination would still fail to render claim 1 unpatentable because the combination fails to disclose each and every claimed element. More specifically, the combination would fail to disclose or suggest a first *gate* redundancy line formed on the interlayer insulating layer, and connected electrically with one of the gate electrode, the gate line, and both the gate electrode and gate line through a first gate contact hole and formed of the same material as one of the source and drain electrodes.

Independent claim 8 defines an array substrate that includes *inter alia*, a gate redundancy line formed on a passivation layer, and connected electrically with one of the gate electrode, the gate line, and both the gate electrode and gate line through a gate contact hole and formed of the same material as the pixel electrode. Independent claim 8 is patentably distinguishable over the combination of Song and Ozaki for at least the reason that the combination fails to disclose each and every claimed element. More specifically, the combination fails to disclose or suggest a gate redundancy line formed on a passivation layer and being of the same material as the pixel electrode as claimed.

Independent claims 14 and 24 define a method of fabricating an array substrate as define

in claims 1 and 8 respectively. Therefore, claims 14 and 24 are patentably distinguishable over the combination of Song and Ozaki for at least those reasons presented above with respect to claims 1 and 7.

Furthermore, claims 2-5, 7, 9-13, 15-19, 23 and 25-30 variously depend from independent claims 1, 8, 14 and 24. Therefore, claims 2-5, 7, 9-13, 15-19, 23 and 25-30 are patentably distinguishable over the combination of Song and Ozaki for at least those reasons presented above with respect to claims 1, 8, 14 and 24. Accordingly, Applicants respectfully request reconsideration and withdrawal of the rejection of claims 1-5, 7-19, and 23-30 under 35 U.S.C. §103(a).

In paragraph 3 of the Action, the Examiner rejects claims 6 and 20-22 under 35 U.S.C. §103(a) as allegedly being unpatentable over Song in view of Ozaki, further in view of U.S. Patent No. 6,307,216 of Huh et al. ("Huh"). Applicants respectfully traverse this rejection.

Claims 6 and 20-22 variously depend from independent claims 1 and 14. Therefore, claims 6 and 20-22 are patentably distinguishable over the combination of Song and Ozaki for at least those reasons presented above with respect to claims 1 and 14. Huh discloses thin film transistor panels for liquid crystal displays that include a data line redundancy structure to effectively repair disconnection defects in the data lines. However, Huh fails to overcome the deficiencies of Song and Ozaki.

Since Song, Ozaki and Huh each fail to disclose or suggest an array substrate comprising a first gate redundancy line formed on the interlayer insulating layer and connected electrically with on of the gate electrode, the gate line, and both the gate electrode and gate line through a first gate contact hole and formed of the same material as one of the source and drain electrodes as claimed, the combination of these three references cannot possibly disclosure said element. Therefore, even if one skilled in the art were motivated to combine Song, Ozaki and Huh, which

Applicants do not concede, the combination would still fail to render claims 6 and 20-22 unpatentable for at least the reason that the combination fail to disclose each and every claimed element. Accordingly, Applicants respectfully request reconsideration and withdrawal of the rejection of claims 6 and 20-22 under 35 U.S.C. §103(a).

The application is in condition for allowance. Notice of same is earnestly solicited. Should the Examiner find the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at (202) 496-7500 to discuss the steps necessary for placing the application in condition for allowance. All correspondence should continue to be sent to the below-listed address.

If these papers are not considered timely filed by the Patent and Trademark Office, then a petition is hereby made under 37 C.F.R. §1.136, and any additional fees required under 37 C.F.R. §1.136 for any necessary extension of time, or any other fees required to complete the filing of this response, may be charged to Deposit Account No. 50-0911. Please credit any overpayment to deposit Account No. 50-0911. A duplicate copy of this sheet is enclosed.

Dated: May 26, 2005

Respectfully submitted,

By Penny L Caudle

Penny L. Caudle
Registration No.: 46,607
MCKENNA LONG & ALDRIDGE LLP
1900 K Street, N.W.
Washington, DC 20006
(202) 496-7500
Attorney for Applicants